

## PART 1

### REFERENCE INFORMATION

#### CONTROL DATA 6400 SYSTEMS CENTRAL PROCESSOR MONITOR

In CONTROL DATA® 6400 Computer Systems, system functions are normally handled by the Monitor located in a Peripheral and Control Processor. The 6400 Computer Systems are equipped with certain hardware capabilities to effectively implement Monitor activities in the Central Processor. Since the Central Processor can reference Extended Core Storage directly for service routines, programs and data, a Central Processor Monitor program to handle these and other functions is faster and more efficient than a Monitor residing in a Peripheral and Control Processor.

The hardware elements of a 6400 System which provide the essential capabilities for implementing a Central Processor Monitor are described in the ensuing paragraphs.

#### MONITOR ADDRESS REGISTER

Contained in the Exchange Jump package (bits 36-53 of location "n+6") is an 18-bit Monitor Address. Just as other Central Processor operational registers are loaded during an Exchange operation, so is the Monitor Address register loaded with the 18-bit Monitor Address. This Monitor Address is the starting address of the Exchange package for an ensuing Central Exchange Jump instruction (except when the Monitor Flag bit is set; refer to the instruction description).

#### MONITOR FLAG BIT

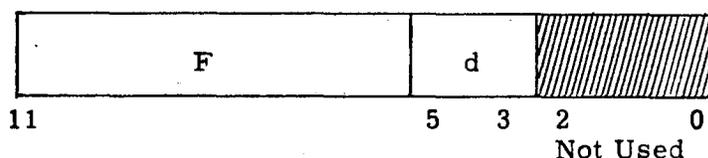
The Central Processor has, in the Central Memory control section of the system, a Monitor Flag bit. A Master Clear (Dead Start) clears the Monitor Flag bit. Any action thereafter on this bit is via the Monitor Exchange or the Central Exchange Jump instructions. (There is no instruction with which to sample the status of this bit directly and/or independently of these instructions.) The operation of this Monitor Flag bit is described under the instruction descriptions.

## MONITOR AND CENTRAL EXCHANGE JUMP INSTRUCTIONS

Two instructions exist for Central Processor monitor implementation: one executable by the Peripheral Processors; the other executable by the Central Processor. These instructions are as detailed below.

### Peripheral Processors

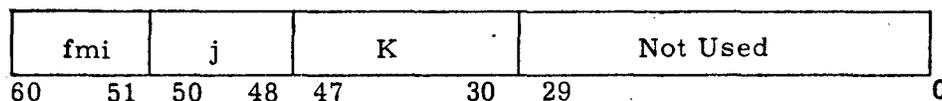
261 MEJ Monitor Exchange Jump (12 bits)



This instruction, typically used to initiate Central Processor Monitor activity, is a conditional exchange jump to the Central Processor. If the Monitor Flag bit is clear, this instruction sets the flag and initiates the exchange. If the Monitor Flag bit is set, this instruction acts as a Pass instruction. The starting address for this exchange is the 18-bit address held in the Peripheral Processor A register. (The Peripheral Processor program must have loaded A with an appropriate address prior to executing this instruction.) Note that this starting address is an absolute address.

### Central Processor

013 CEJ jK Central Exchange Jump (60 bits)



This instruction unconditionally exchange jumps the Central Processor, regardless of the state of the Monitor Flag bit. Instruction action differs, however, depending on whether the Monitor Flag bit is set or clear. Operation is as follows:

- a) Monitor Flag bit clear. The starting address for the exchange is taken from the 18-bit Monitor Address register. Note that this starting address is an absolute address. During the exchange, the Monitor Flag bit is set.

- b) Monitor Flag bit set. The starting address for the exchange is the 18-bit result formed by adding K to the contents of register Bj. Note that this starting address is an absolute address. During the exchange, the Monitor Flag bit is cleared.

Table 1 summarizes the operational differences between the normal Exchange Jump instruction (260) and the Monitor and Central Exchange Jumps (261 and 013)

TABLE 1-1. EXCHANGE INSTRUCTION DIFFERENCES

INSTRUCTION	CONDITIONAL/ UNCONDITIONAL	OPERATIONAL DIFFERENCES	
		Effect on Monitor Flag Bit	Location of Starting Address for Exchange
260 (Normal Peripheral Processor Exchange Jump)	Unconditional	No effect on Flag	Peripheral Processor A Register
261 (Peripheral Processor Monitor Exchange Jump)	Conditional (occurs only if Monitor Flag bit is clear; Passes if Flag is set)	Sets Flag	Peripheral Processor A Register
013 (Central Exchange Jump) with Monitor Flag Bit clear	Unconditional	Sets Flag	Central Processor Monitor Address Register
013 (Central Exchange Jump) with Monitor Flag Bit set	Unconditional	Clears Flag	Address formed by $K+(B_j)$

## PROGRAMMING NOTES

- 1) The Exchange package is precisely as described in the 6400/6500/6600 Computer Systems Reference manual (Publication No. 60100000) with the single exception that bits 36-53 of location "n+6" hold a Monitor Address. Note that any exchange (260, 261, or 013) to that package will load the contents of location "n+6" into the Monitor Address register (other operational registers are similarly loaded). Thus, any ensuing 013 instruction using the contents of the Monitor Address register as a starting address uses those contents as loaded.
- 2) The Exchange packages for entering the Central Processor Monitor should usually have the Reference Address (RA) equal to 000000 and the Field Length (FL) equal to Central Memory size.
- 3) Since the Monitor Flag bit cannot be directly sampled, a program cannot directly determine its state; hence, success in performing a Peripheral Processor Monitor Exchange cannot readily be predicted. Further, program control always is given to the next instruction, whether or not the Exchange is honored. A method of determining whether the Monitor Exchange occurred is as follows:
  - a) Set Bo (bits 0-17 of location "n") in the Exchange package to 7777
  - b) Initiate the Monitor Exchange (261)
  - c) Read Bo from the Exchange package in Central Memory.  
If the Monitor Exchange was honored, Bo in the Exchange package will equal 000000. If the instruction passed, this location still holds 7777.
- 4) Different Exchange packages should be used for Central Processor exchanges and Peripheral Processor exchanges. This aids software determination of which of two jumps (Central or Monitor Exchange Jumps) was executed when both were initiated at approximately the same time.

- 5) Simultaneous Exchange requests are resolved in favor of the Central Processor.
- 6) If either a 260 or 261 instruction are waiting to be honored when the Central Processor issues an 013 K instruction, the 013 instruction is not executed and the Peripheral Processor Exchange occurs. When control is returned to the exchanged program (the interrupted program containing the 013<sub>j</sub>K instruction), the 013<sub>j</sub>K instruction is re-issued and executed.
- 7) The state of the Monitor Flag bit has no effect on the operation of the normal PP Exchange Jump (260); nor has this instruction any effect on the Flag.